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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,307	02/10/2004	Ching-Nan Hsiao	10113741	1517
34283	7590	09/21/2006	EXAMINER	
QUINTERO LAW OFFICE 1617 BROADWAY, 3RD FLOOR SANTA MONICA, CA 90404			THOMAS, TONIAE M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/775,307	<b>Applicant(s)</b> HSIAO ET AL.	
	<b>Examiner</b> Toniae M. Thomas	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>05/12/06</u> . | 6) <input checked="" type="checkbox"/> Other: <u>See Continuation Sheet</u> .           |

Continuation of Attachment(s) 6). Other: copy of PTO 892 from action mailed 24 Aug 2005 .

**DETAILED ACTION**

1. This action is in response to the reply filed on 27 June 2006.
2. Currently, claims 1-12 are pending.

***Information Disclosure Statement***

3. The information disclosure statement filed on 12 May 2006 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language.

Therefore, the foreign reference, CN 1189919 A, listed as citation B1 in the IDS filed on 12 May 2006 has not been considered. In addition, please note that the US Patent reference, US 5,315,142 (Acovic et al.), listed as citation A1 in the IDS has also not been considered because the examiner previously cited the patent in the Office action mailed on 24 August 2005 (a copy of the PTO 892 form mailed with the Office action is attached hereto).

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 as submitted in the amendment filed on 27 June 2006 recites the limitation "forming a conducting layer over the insulating layer and filling the trench" (claim 1, line 9). The phrase "the insulating layer" lacks antecedent basis. It is unclear which insulating layer the phrase is referring to: the bit line insulating layers, or the conformable oxide layer.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. (US 2004/0130934 A1).

The Prall et al. application publication (referred to hereinafter as Prall) discloses a method for fabricating an NROM memory cell (see figs. 1, 2 and accompanying text). The method comprises: providing a semiconductor substrate having a trench 22 (fig. 1 and par. 0046); forming doped areas 24, 26, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench (fig. 1 and par. 0046); forming bit line insulating layers 28, 32, 42 over each of the doping areas (fig. 1 and par. 0047, lines 3-6; fig. 2 and par. 0049, lines 1-7); forming a conformable insulating layer 44 over a

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sidewall of the trench and the bit line insulating layers to locally store electric charge (fig. 2 and par. 0051, lines 4-10); and forming a conducting layer 38 over the insulating layer and filling in the trench (fig. 2 and par. 0048, lines 7-8).

The bit line insulating layers 32, 42 are formed by thermal oxidation (par. 0049, lines 1-5).

The conformable oxide layer is a silicon rich oxide layer ().

The thickness of the conformable oxide layer is 50 to 110 Å ().

A gate dielectric layer, thin oxide layer 42, is formed between the conformable insulating layer and the trench surface (fig. 2 and par. 0051, lines 1-4).

The thickness of the gate dielectric layer is.

The conducting layer 38 is a poly layer (par. 0048, lines 7-8).

While Prall discloses forming a conformable insulating layer 44 to locally store charge, Prall does not teach that the conformable insulating layer is a conformable oxide layer, or that the conformable oxide layer is a Si-rich oxide layer.

Forbes discloses a method for forming a multi-state NROM device.

Forbes lists several insulating materials that may be used as a charge storing or charge trapping layer in multi-state NROM devices (par. 0046, lines 4-15).

These materials include silicon nitride and Si-rich oxide (par. 0046, lines 9-10).

The conformable charge storing insulating layer 44 in Prall is a silicon nitride layer. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a Si-rich oxide layer in place of the nitride layer for the conformable insulating layer, because Si-rich oxide films are charge storage films that can be used for storing charge in multi-state memory cell devices.

Forbes does not teach forming the Si-rich oxide layer to a thickness of 50 to 110 Å. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the Si-rich oxide layer to a thickness of 50 to 110 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233).

Prall does not teach that the bit line insulating layers are formed to a thickness of 300 to 2000 Å, or that the gate dielectric layer is formed to a thickness of 50 Å. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the bit line insulating layers to a thickness of 300 to 2000 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233). Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the gate dielectric layer to a thickness of 50 Å, since it has been held that discovering an

optimum value of a result effective variable involves only routine skill in the art (*In re Boesch*, 205 USPQ 215 (CCPA 1980)).

### **Conclusion**

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT

16 September 2006



M. Wilczewski  
Primary Examiner  
TC 2800